CLAIMS

1. A method of simulating a circuit using an analog or RF simulator, comprising:

defining two circuit descriptions to be used during the simulation, a first circuit description used for accuracy of the simulation and a second circuit description, different from the first circuit description, used for increasing the speed of the simulation; and

simulating the circuit using both the first and second circuit descriptions.

2. The method of claim 1, wherein the first circuit description includes parasitic information and the second circuit description has the parasitic information removed or substantially reduced.

3. The method of claim 1, further including reading a netlist including parasitic information or reading a netlist and a separate file containing parasitic information, and wherein the first circuit description includes all of the elements included in the netlist plus the parasitic information.

4. The method of claim 3, further including modifying the first circuit description to generate the second circuit description with reduced parasitic information, wherein modifying includes:

analyzing values and functionality of electrical components in the circuit to determine which components are parasitic information; and

removing the parasitic information based on the analysis.

5. The method of claim 3, further including modifying the first circuit description to generate the second circuit description with reduced parasitic information, wherein modifying includes:

identifying circuit components marked as parasitic information; and

removing the parasitic information based on the identification.

6. The method of claim 1, wherein simulating includes solving a system of interrelated equations, wherein a part of the system of equations uses the first circuit description and wherein a part of the system of equations uses the second circuit description.

7. The method of claim 1, further including:

forming a first list including circuit components without parasitic information;

forming a second list including the parasitic information;

forming first and second simulation data structures using the first and second lists, respectively; and

wherein the first circuit description is defined as a combination of the first and second lists, and the second circuit description is defined as only the first list.

8. The method of claim 7, further including evaluating $F(X^i)$ using both the first and second simulation data structures for accuracy and performing a factorization of a Jacobian matrix built using only the first simulation data structure for increasing the speed of the simulation.

9. The method of claim 1, wherein simulating includes solving a form of the equation $J\Delta X = -F(X^i)$ wherein J is a Jacobian matrix related to the circuit components, $F(X^i)$ is an evaluated equation, and ΔX is a variable to be solved, and further including factorizing the matrix J built using the second circuit description, evaluating $F(X^i)$ using the first circuit description and solving for ΔX.

10. The method of claim 1, wherein the analog simulation is used for any one or more of the following: DC, AC, and transient analysis and the RF simulation is used for state-state analysis and modulated steady-state analysis.

11. The method of claim 1, wherein simulating further includes factorizing a Jacobian matrix built using the second circuit description for preconditioning a linear iterative solver.

12. The method of claim 1, further including receiving, on a server computer, a circuit description from a client computer over a distributed network, simulating the description on the server computer, and returning simulation results to the client computer over the distributed network.

13. An analog or RF simulator for simulating a circuit, comprising:

an elaboration engine that receives one or more lists associated with the circuit including a list of components in the circuit, interconnections between the components, and parasitic information and that defines two circuit descriptions, a first circuit description used for accuracy of the simulation and a second circuit description used for speed of the simulation, the first circuit description being different from the second circuit description; and

a simulation kernel coupled to the elaboration engine that includes at least a direct solver or linear iterative solver to simulate the circuit, wherein the simulation kernel solves a system of equations, part of the system of equations using the first circuit description and part of the system of equations using the second circuit description.

14. The analog simulator of claim 13, further including a preconditioner coupled to the linear iterative solver.

15. The analog simulator of claim 14, wherein the one or more lists include a netlist and a DSPF, including parasitic information.

16. The analog simulator of claim 13, wherein the simulation kernel evaluates $F(\underline{X}^i)$ using the first circuit description and performs a factorization of a Jacobian matrix J using the second circuit description to solve an equation $J\Delta X = -F(X^i)$.

17. The analog simulator of claim 13, further including a network coupled to the simulator through which the first circuit description is received.

18. A simulator for simulating a circuit, comprising:

means for reading a first description of the circuit that includes a list of components in the circuit, the interconnections between the components, and parasitic information;

means for generating a second circuit description by removing at least a part of the parasitic information from the first circuit description; and

means for simulating the circuit using substantially the first circuit description including the parasitic information and the second circuit description with reduced parasitic information.

19. The simulator of claim 18, further including means for solving a linear system of equations using an iterative solver or a direct solver.

20. The simulator of claim 18, wherein the means for simulating includes evaluating $F(\underline{X}^i)$ using the first circuit description and factorizing a Jacobian matrix J using the second circuit description to solve an equation $J\Delta X = -F(X^i)$.

21. A method of simulating a circuit using an analog or RF simulator, comprising:

generating a system of equations wherein a part of the system of equations uses a first circuit description including parasitic information and a part of the

system of equations uses a second circuit description with parasitic information removed;

solving the system of equations in order to simulate the circuit; and

outputting the simulation results.

22. The method of claim 21, wherein generating the system of equations includes solving a form of the equation $J\Delta X = -F(X^i)$ wherein J is a Jacobian matrix related to the circuit components, $F(X^i)$ is an evaluated solution, and ΔX is a variable to be solved.

23. The method of claim 22, wherein solving further includes factorizing the Jacobian matrix J using the modified circuit description, evaluating $F(X^i)$ using the first circuit description, and solving for ΔX.